CPER – Comité de suivi EE4.0 Développement d'un outil d'études de stabilité des simulations de type PHIL – Bilan bibliographique et planning de travail

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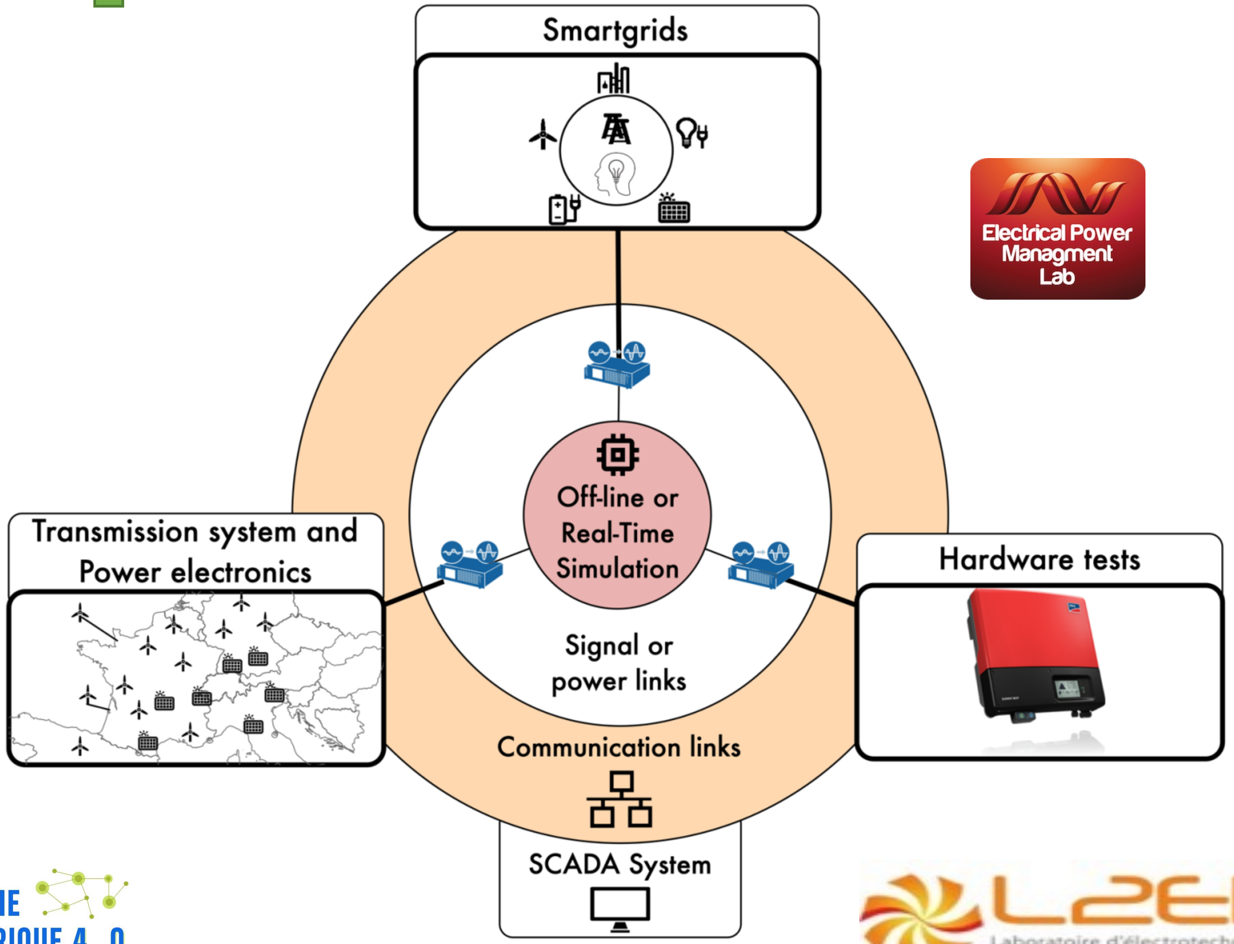
EPMLab – General description

Open R&D environnement in the field of new types of energy conversion, generation and storage integration in power system based on **off-line and real time simulation.**

2 scientific skills

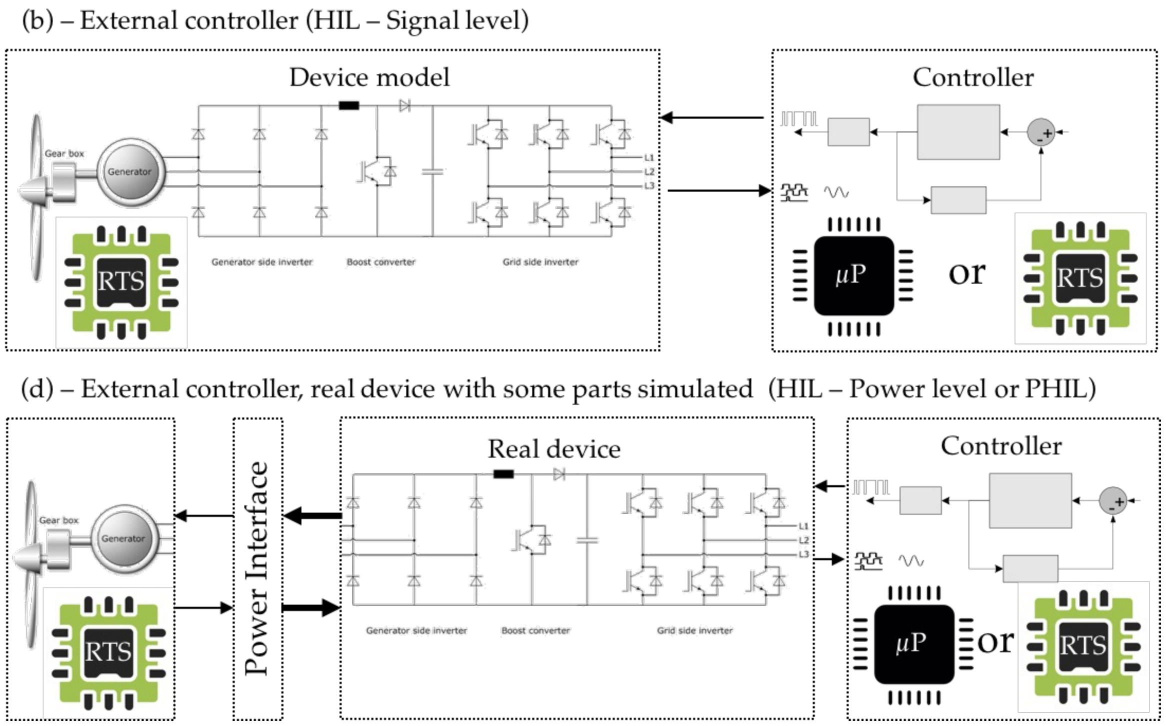
- ✓ **Transmission system and power electronics**
- ✓ **Smart grids**

Test of grid-connected hardware



HIL/PHIL

- **The core of EPMLab is based on RT simulation which allows to carry out HIL and PHIL applications. This allows to study real hardware connected in their emulated environment**



General introduction

- **Les travaux présentés ici sont issus des travaux d'Etienne Auzeral**

- **En poste depuis le 8 Janvier 2024 jusqu'en Octobre 2024, continuité en thèse dans le laboratoire ensuite**

- **Objectif global du projet : Développement d'un outil d'analyse de stabilité des boucles PHIL**

- **Objectif de la présentation : Bilan des travaux réalisés depuis Janvier**
  - **Présenter les limites de stabilité des boucles PHIL et les modèles qui seront utilisés pour l'étude de stabilité**

1°) What is PHIL ?

2°) Problem statement

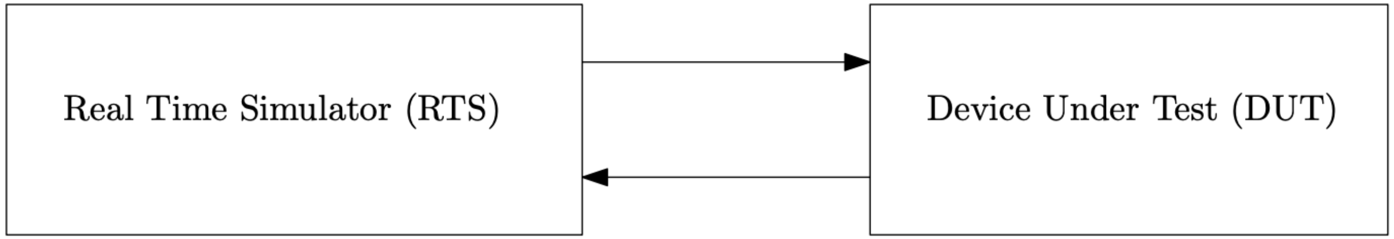
3°) Models studied

- ITM,
- Fast-loop,
- BTLM-PHIL

4°) Futur Works

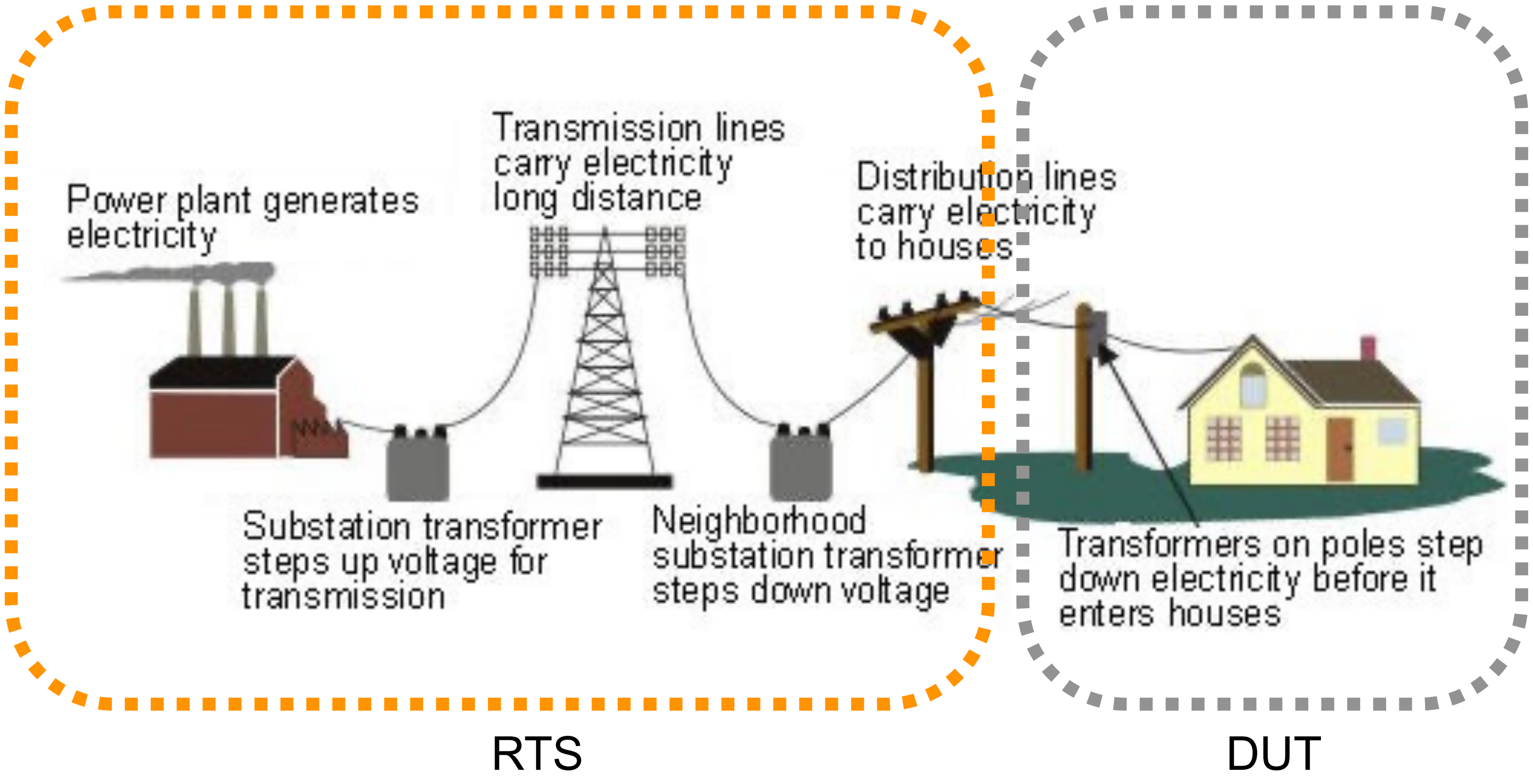
PHIL - Principle

Power Hardware In the Loop (PHIL) is an experimentation where the device tested (DUT) is connected to a simulated environment provided by a real time simulator (RTS).



PHIL: Use cases

- In our cases, RTS will mainly simulate a real-time power grid to validate the design of the DUT.



PHIL

1°) What is PHIL ?

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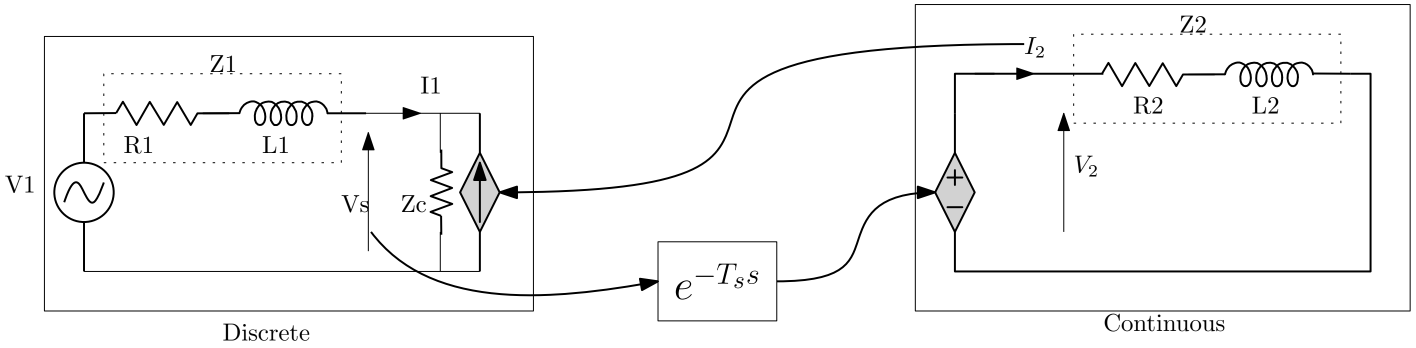
4°) Future Work

PHIL

To study the stability of PHIL, the following model is widely used. A Delay is used to model the connections between the RTS and the DUT



Let's suppose Z1 and Z2 are purely resistive

$$i_1(z) = i_2(z)$$

$$i_1(z) = \frac{v_e(z) - v_1(z)}{Z_1}$$

$$v_2(z) = z.v_1(z)$$

$$v_2(z) = Z_2 i_2(z)$$

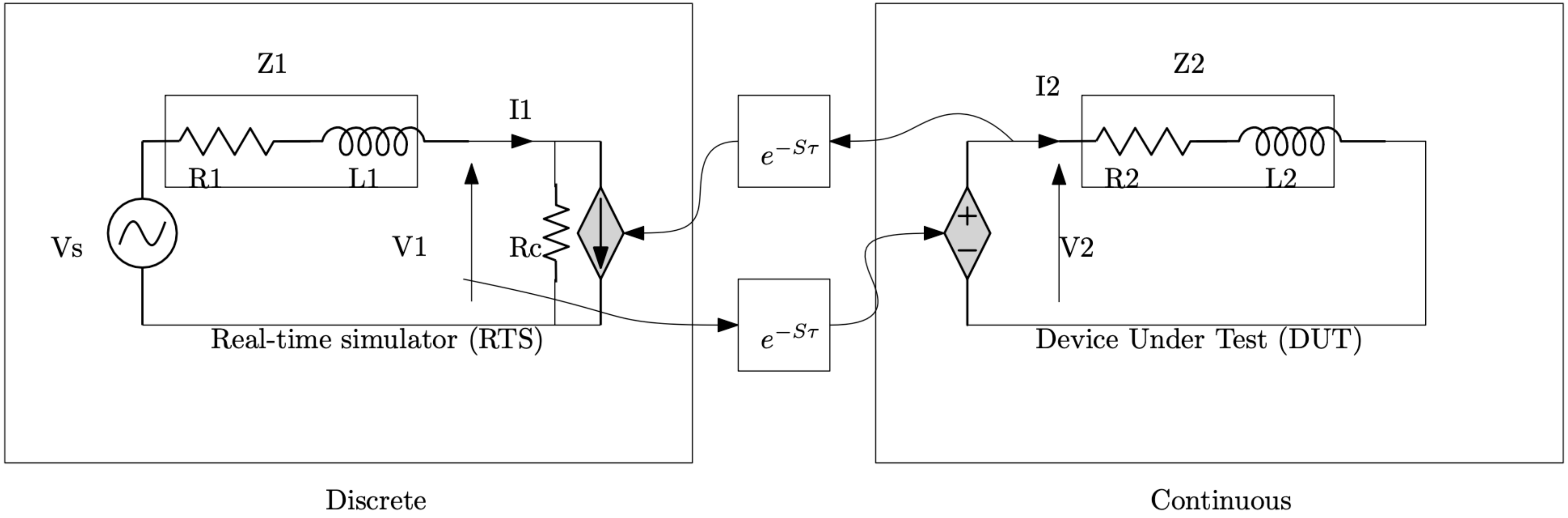
$$\frac{i_1(z)}{v_e(z)} = \frac{1}{Z_1 + z.Z_2}$$

=> Unstable if Z1 > Z2

Extension : A stability study of this model shows that the system is stable when |Z1| < |Z2| at all frequencies.

PHIL

In practice, RTS is discrete, we have to consider :
- the whole system as hybrid (continuous+discrete)
- the delay for the feedback measurement



The stability rule became: |Z1| < 0.5 |Z2|

PHIL: Partial conclusion

- System studied must be considered as Hybrid to show the stability limits

- Delays impact on system stability

- We must know Z2 to design Z1 to be sure that the loop is stable

1°) What is PHIL ?

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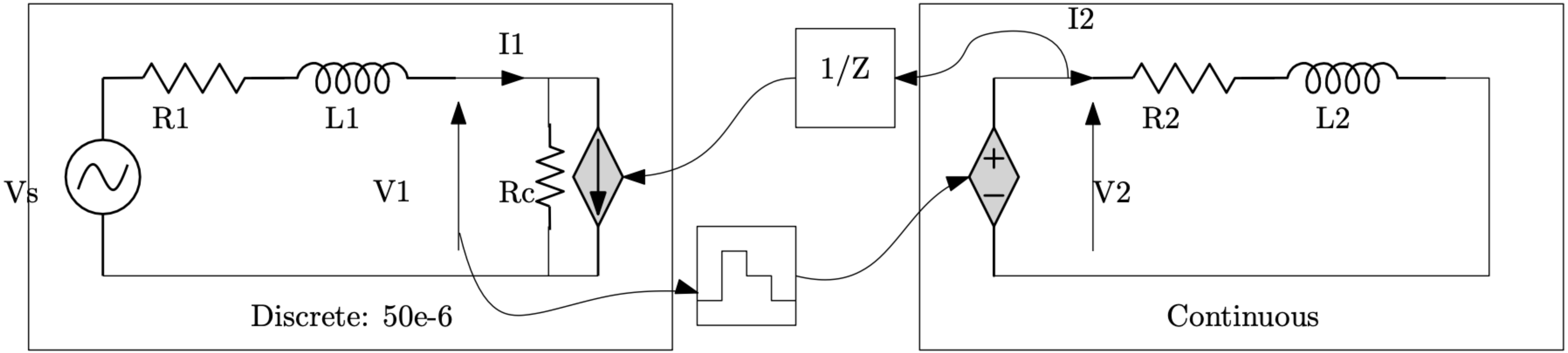
PHIL: Models studied

In this section, we will study in detail the stability of three models:

1°) ITM
2°) Fast-loop
3°) BTLM-PHIL

PHIL: Methods

1°) Ideal Transformer method

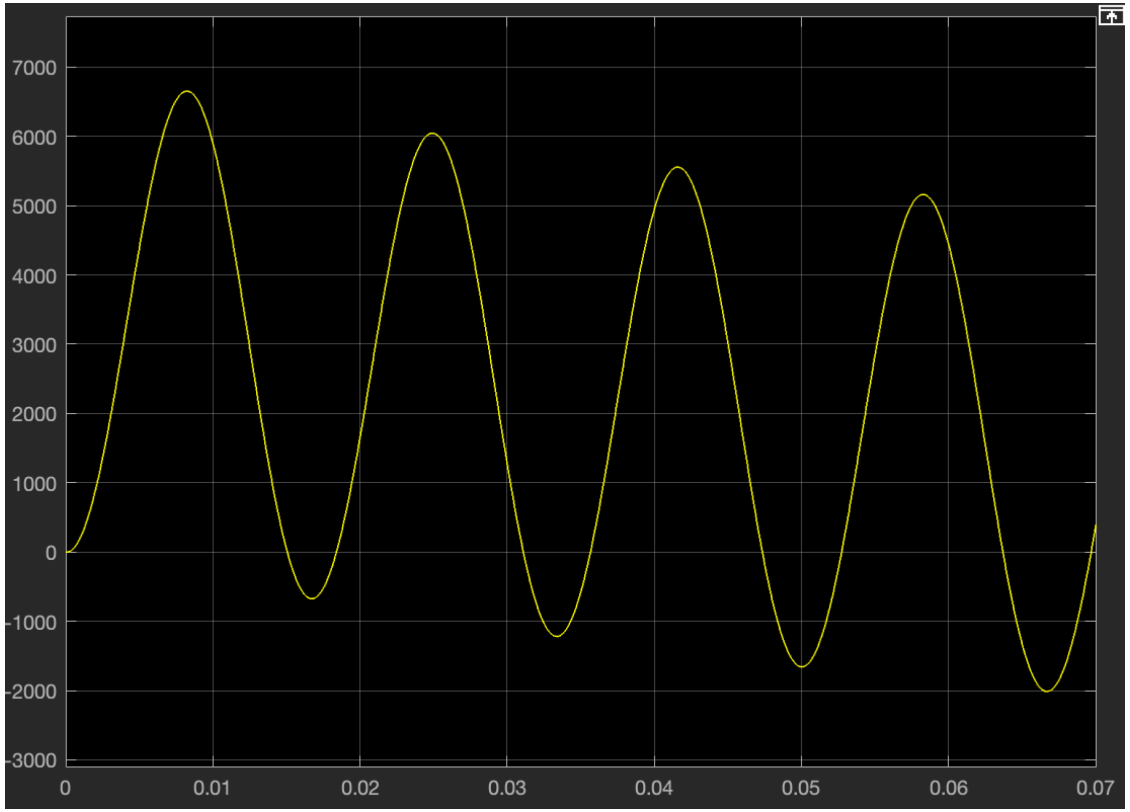


PHIL: Ideal Transformer Method (ITM)

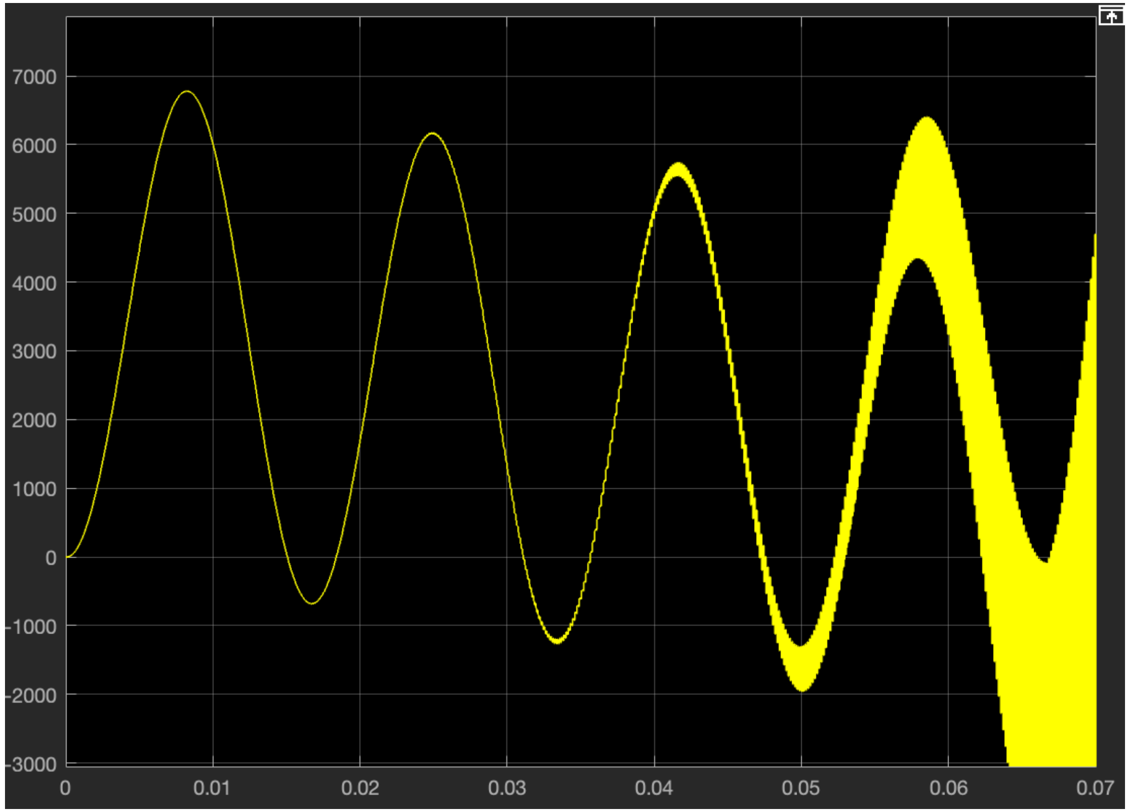
ITM

Ratio	R1	L1	Z1	R2	L2	Z2	Stable ?
0,1	0,0460	0,0036	1,3579	0,4600	0,0360	13,5795	Stable
0,2	0,0460	0,0036	1,3579	0,2300	0,0180	6,7897	Stable
0,49	0,0460	0,0036	1,3579	0,0939	0,0073	2,7713	Stable
0,51	0,0460	0,0036	1,3579	0,0902	0,0071	2,6626	Unstable
0,6667	0,0460	0,0036	1,3579	0,0690	0,0054	2,0368	Unstable
1	0,0460	0,0036	1,3579	0,0460	0,0036	1,3579	Unstable

PHIL: Ideal Transformer Method (ITM)



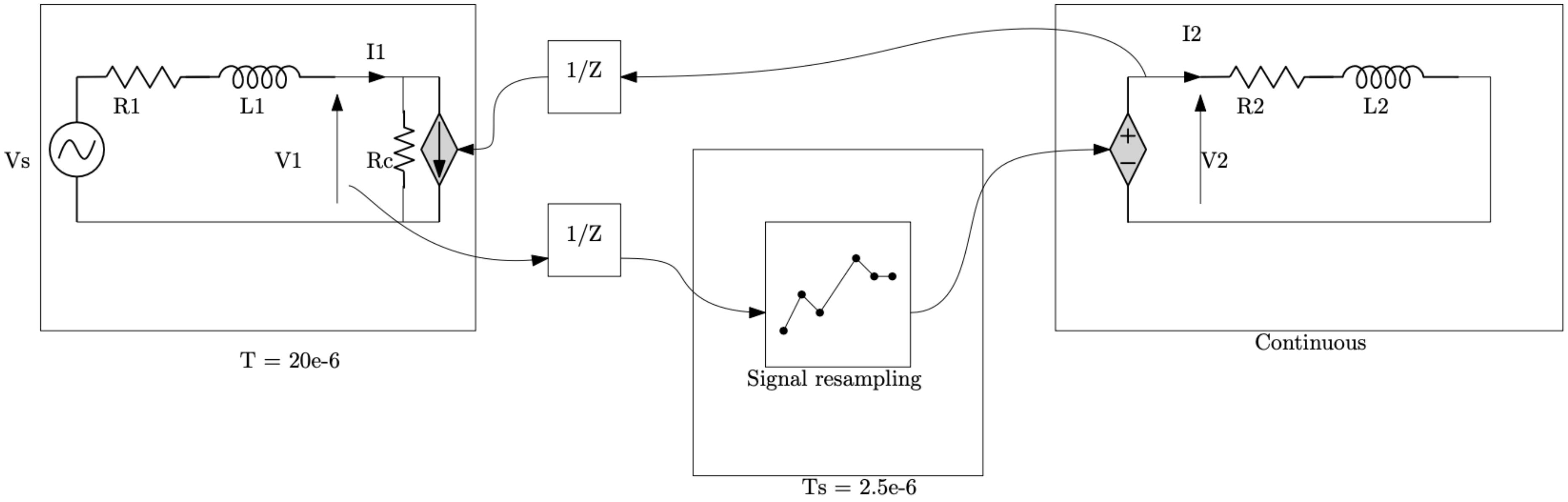
|Z1| = 0.49 |Z2|



|Z1| = 0.51 |Z2|

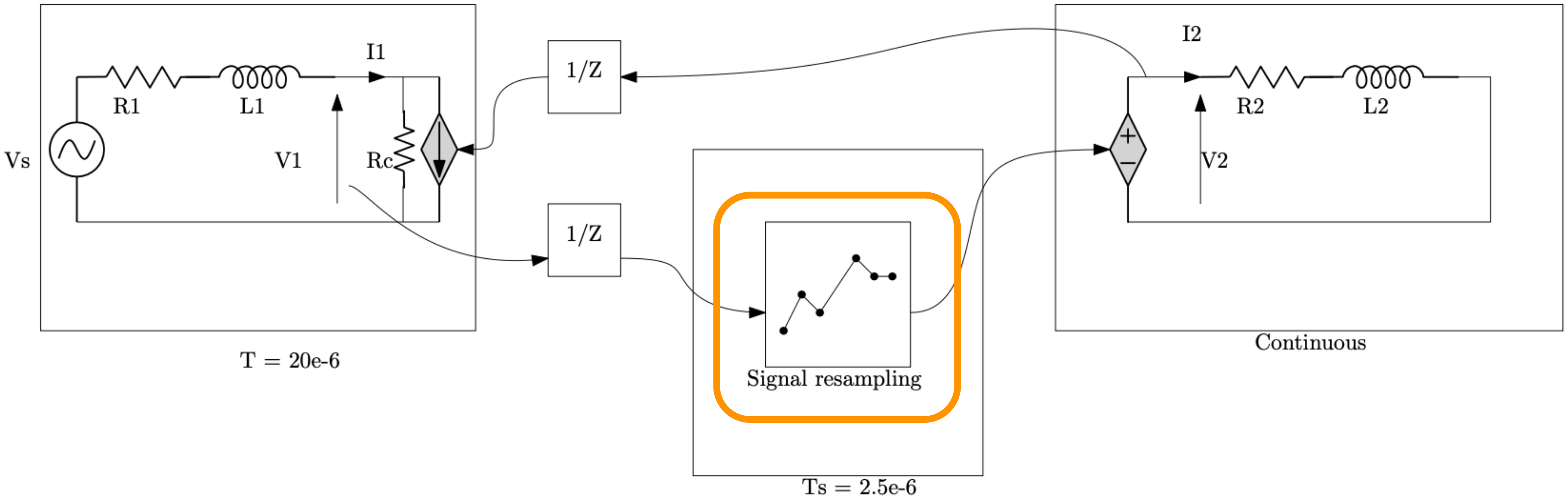
PHIL: Methods

2°) Fast-Loop



PHIL: Methods

2°) Fast-Loop

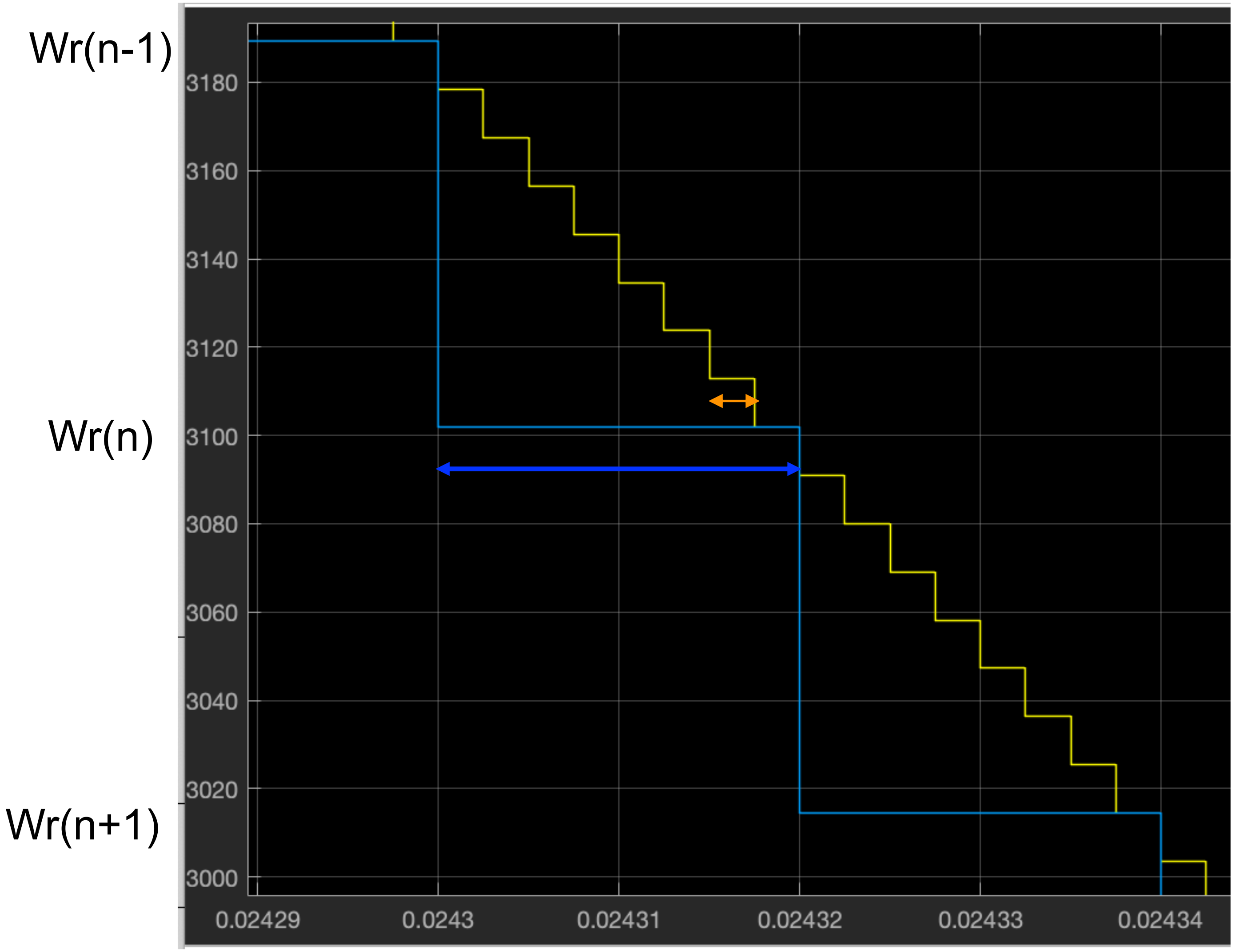


PHIL: Sampling component

Goal:

Input sample signal at Ts (Discrete Time of RTS)

Output sample signal at T (Discrete Time of FPGA)

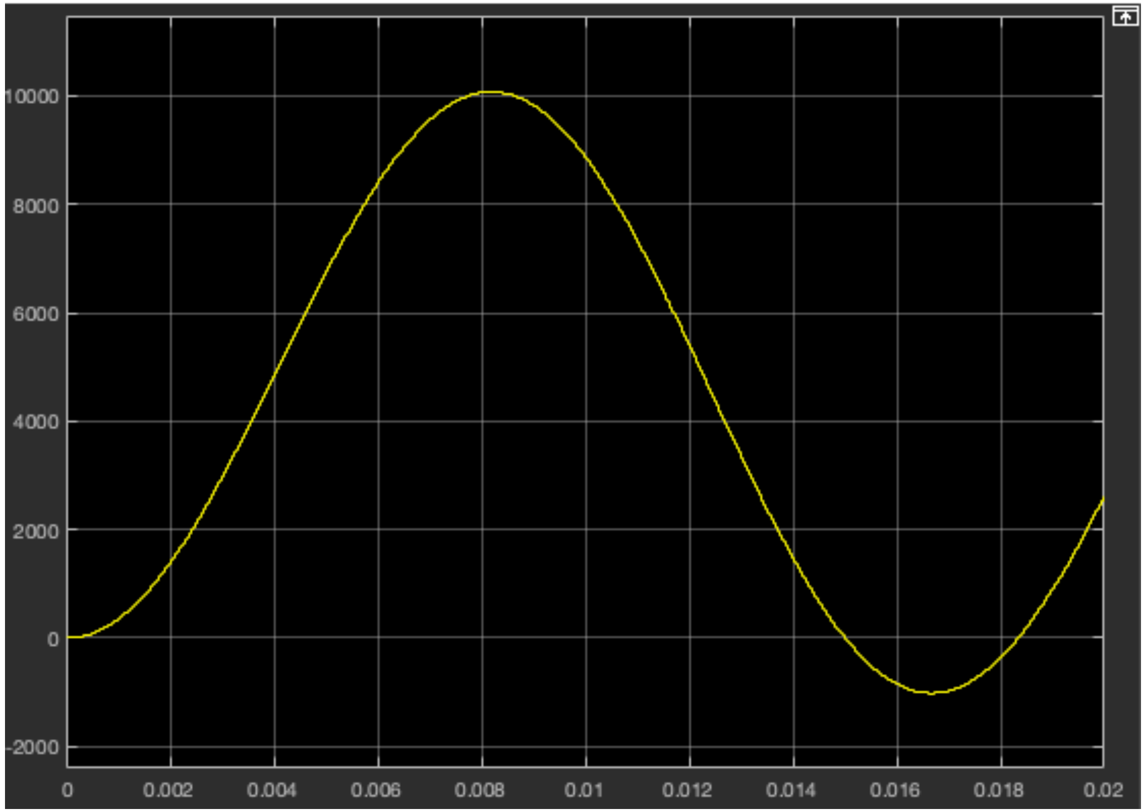


PHIL: Fast-loop

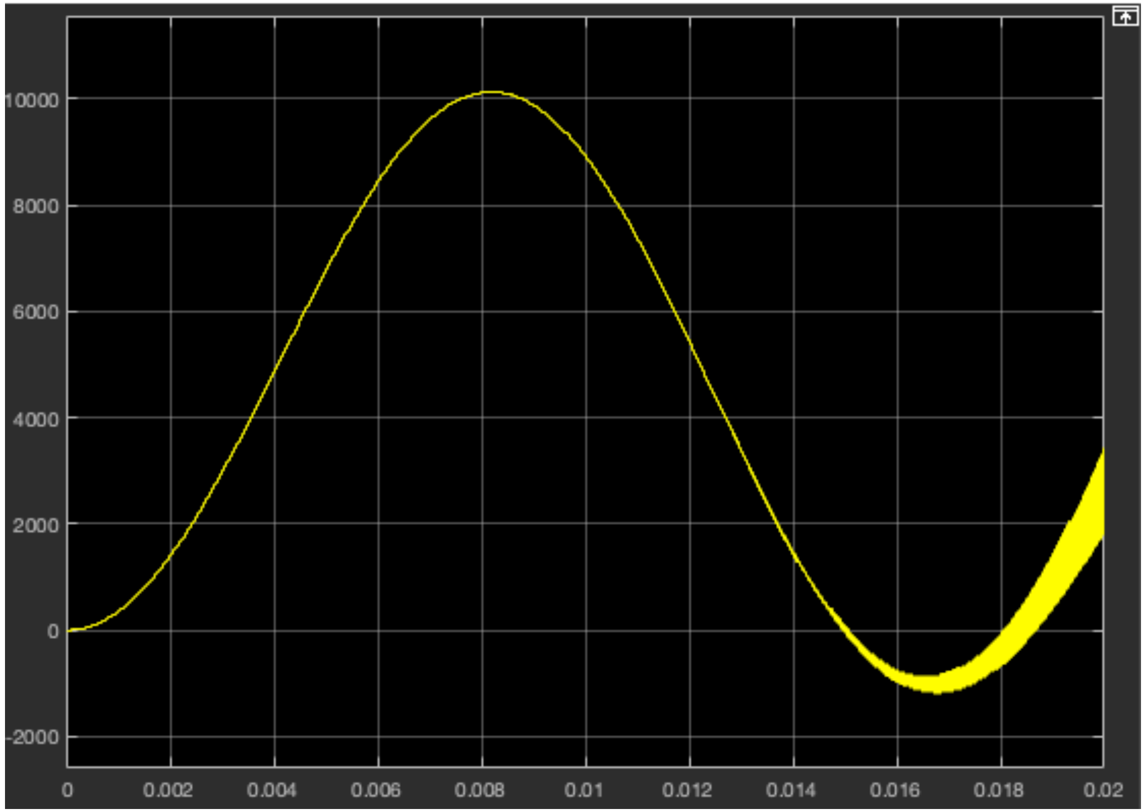
Fast-Loop

Ratio	R1	L1	Z1	R2	L2	Z2	Stable ?
0,1	0,0460	0,0036	1,3579	0,4600	0,0360	13,5795	Stable
0,49	0,0460	0,0036	1,3579	0,0939	0,0073	2,7713	Stable
0,51	0,0460	0,0036	1,3579	0,0902	0,0071	2,6626	Stable
1	0,0460	0,0036	1,3579	0,0460	0,0036	1,3579	Stable
1,01	0,0460	0,0036	1,3579	0,045545	0,003564	1,3445	Unstable

PHIL: Fast-loop



|Z1| = |Z2|

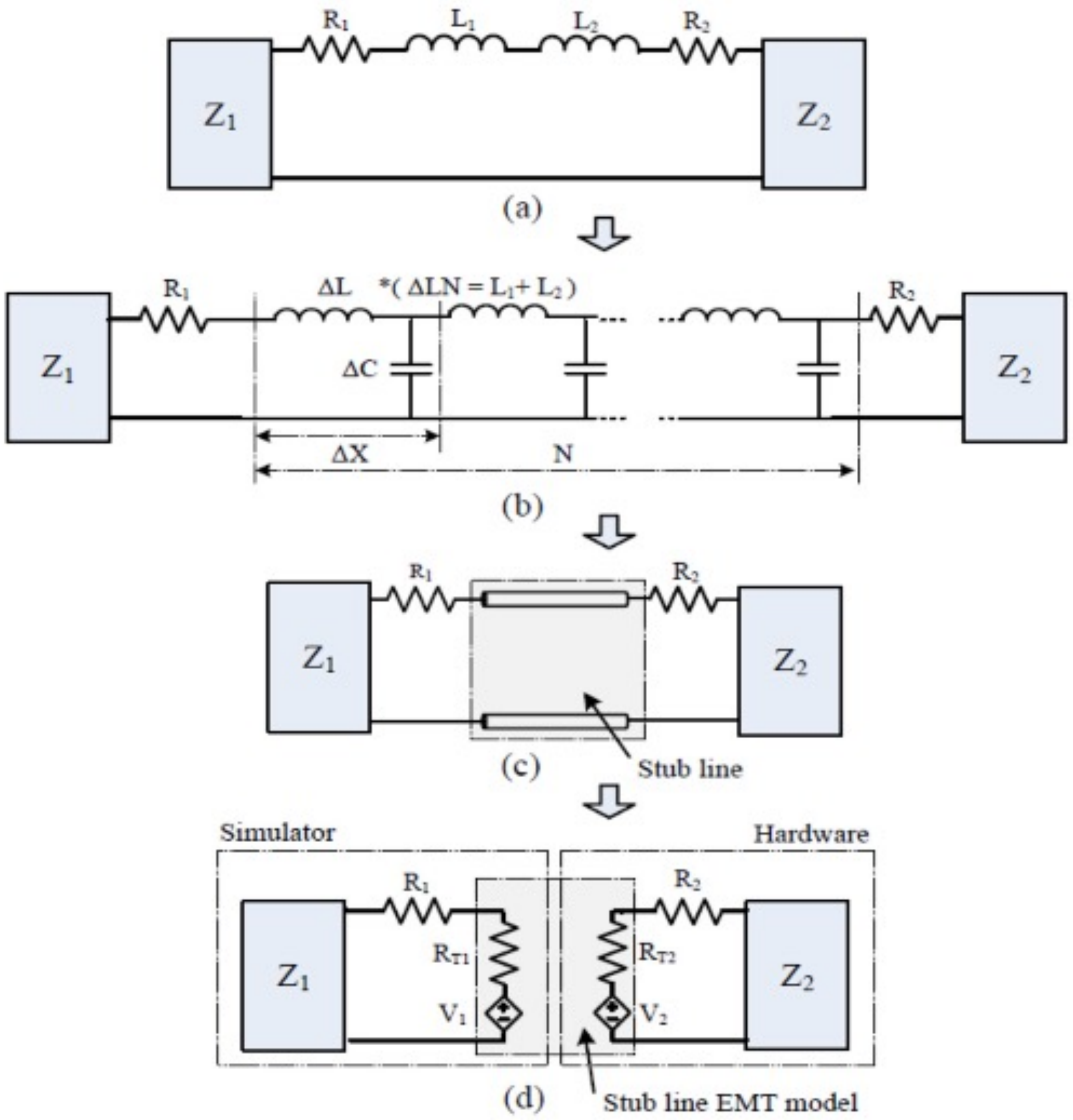


|Z1| = 1.01 |Z2|

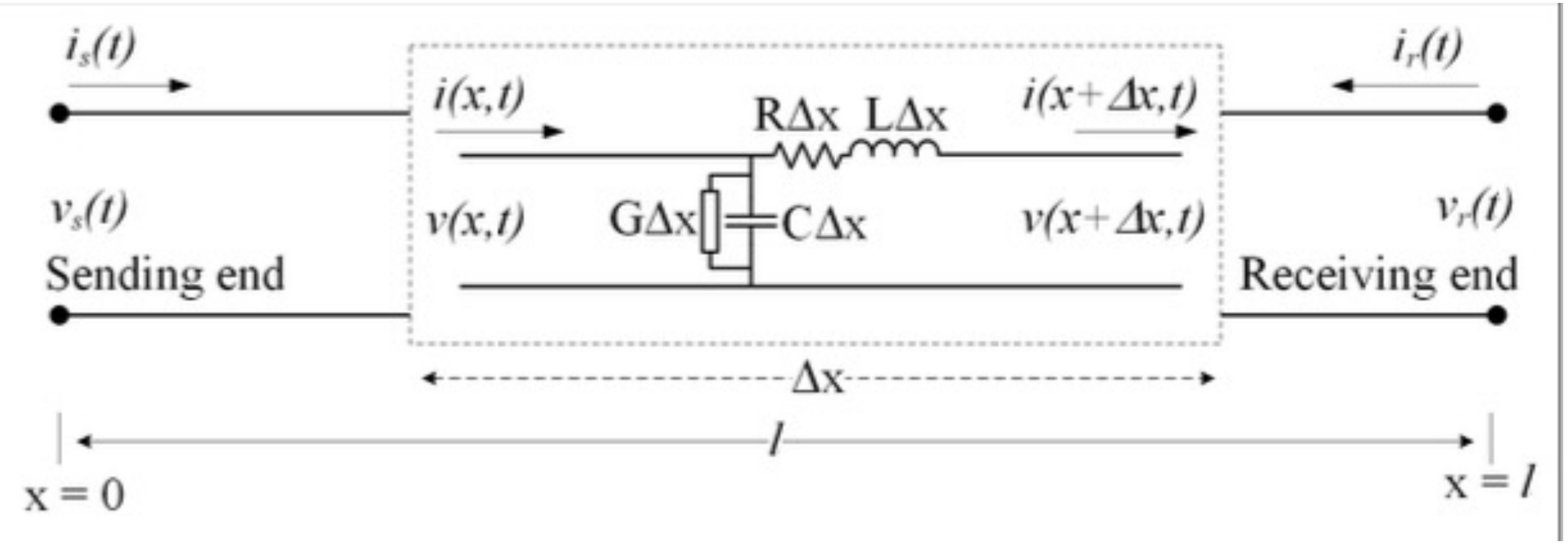
PHIL: BTLM-PHIL

Transmission Line Model:

Using transmission line model allow to parallelize calculation for both sending end and receiving end without introducing any delay error. This method is always numerically stable

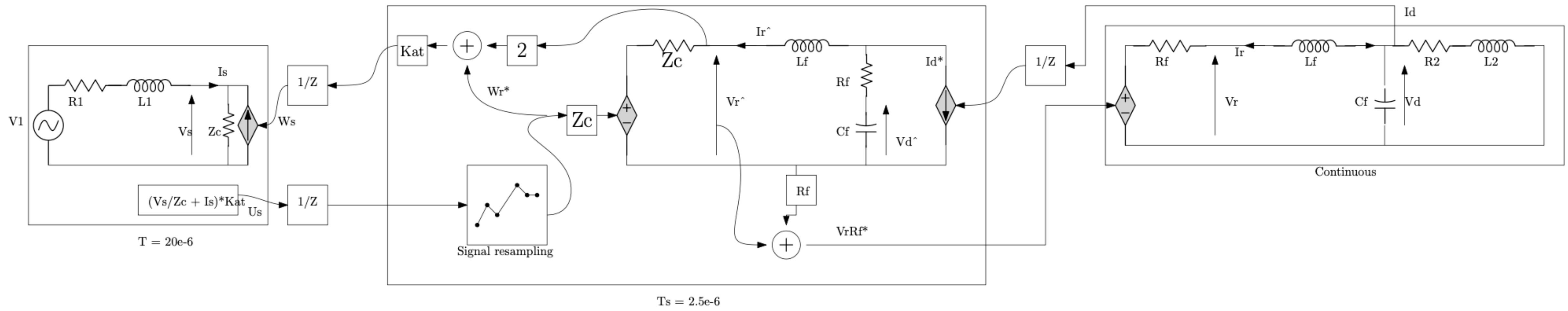


The Telegraph equations



PHIL: BTLM-PHIL

BTLM-PHIL: Bergeron Transmission Line Method:



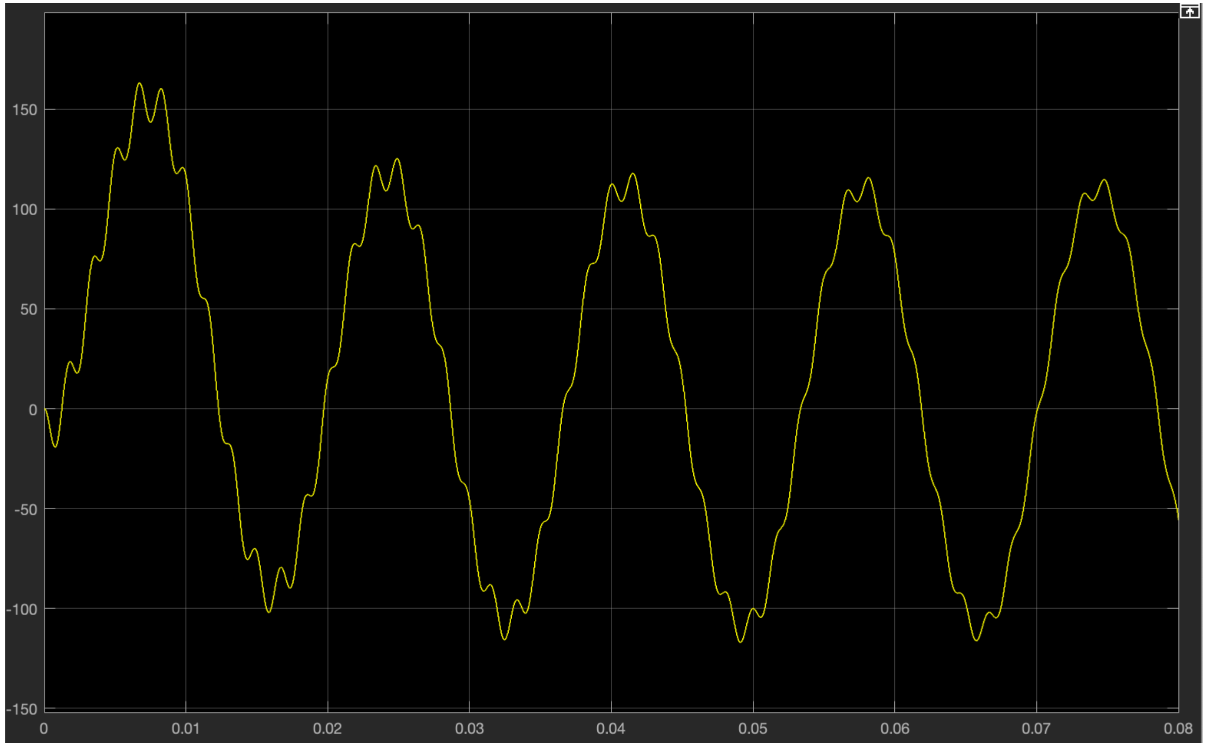
PHIL: BTLM-PHIL

BTLM-PHIL

Ratio	Z2 X/R ratio	Ratio |Z1| / |Z2|	R1	L1	Z1	R2	L2	X2	Z2	Stable ?
0,1	**3,9989**	0,1000	20,74	0,220	85,4919	207,4000	2,2000	829,3805	854,9191	Stable
0,49	**3,9989**	0,4900	20,74	0,220	85,4919	42,3265	0,4490	169,2613	174,4733	Stable
0,51	**3,9989**	0,5100	20,74	0,220	85,4919	40,6667	0,4314	162,6236	167,6312	Stable
1	**3,9989**	1,0000	20,74	0,220	85,4919	20,7400	0,2200	82,9380	85,4919	Stable
3	**3,9989**	3,0000	20,74	0,220	85,4919	6,9133	0,0733	27,6460	28,4973	Stable
5	**3,9989**	5,0000	20,74	0,220	85,4919	4,1480	0,0440	16,5876	17,0984	Stable
(X/R = 0.05)	**0,0500**	0,5144	20,74	0,220	85,4919	166,0000	0,0220	8,2938	166,2071	Stable
(X/R = 0.05)	**0,0500**	1,0287	20,74	0,220	85,4919	83,0000	0,0110	4,1469	83,1035	Stable
(X/R = 0.05)	**0,0500**	2,0575	20,74	0,220	85,4919	41,5000	0,0055	2,0735	41,5518	Stable

PHIL: BTLM-PHIL

|Z1| = 2 |Z2| (X/R = 0.05)



|Z1| = 2 |Z2| (X/R = 4)

=> Advantage of the method: stability

=> Disadvantage: Loss of precision as an interface component has been added

PHIL

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4°) Future Work

- **Rappel de l'objectif global : Développer un outil d'analyse qui permet de prédire si la boucle PHIL va être stable**

- **Prise en main des méthodes d'études de stabilité dans le domaine discret**
  - **Stabilité et transformée en z**
  - **Etude en multirate**
- **Application sur les méthodes présentées**
- **Détermination de l'endroit optimal ou des paramètres optimaux de l'interface permettant de garantir la stabilité ainsi qu'une précision « acceptable »**